Claims

We claim:

1. A method for error protection of a cache memory, wherein each entry in the tag memory and data store within the cache memory associates with a parity bit, comprising:

(a) providing a read request to a system memory associated with the cache memory, the read request correlating to an entry in the tag memory and the data store;

(b) checking the parity bit associated with the correlated entry in the tag memory and the parity bit associated with the correlated entry in the data store; and

(c) if either act (a) or act (b) indicates an error in the corresponding correlated entry, declaring a miss.

2. The method of claim 1, wherein the cache memory is a second level cache.

3. The method of claim 1, further comprising invalidating the correlated entry in the data store if a miss is declared in act (c).

4. The method of claim 3, wherein act (b) comprises:

checking the parity bit associated with the correlated entry in the tag memory; and

if the parity bit associated with the correlated entry in the tag memory indicates no error:

determining if the correlated entry in the tag memory indicates a hit; and

if there is a hit, checking the parity bit associated with the correlated entry in the data store.

5. The method of claim 4, further comprising:

if the parity bit associated with the correlated entry in the data store indicates no error, retrieving the correlated entry from the data store.

6. The method of claim 5, wherein the retrieving the correlated entry from the data store act comprises retrieving the data line containing the correlated entry.

7. A cache, comprising:

a data store;

a tag memory; and

a parity bit memory configured to store a parity bit for each entry in the data store and for each entry in the tag memory.

8. The cache of claim 7, wherein each entry in the data store has a corresponding entry in the tag memory and wherein the parity bit stored for each entry in the data

store is independent from the parity bit for the corresponding entry in the tag memory.

9. The cache of claim 7, wherein each entry in the data store has a corresponding entry in the tag memory and wherein the parity bit memory is configured to store a single parity bit for each data store entry and its corresponding tag memory entry.

10. The cache of claim 7, wherein the cache is configured as a write-through cache.

11. The cache of claim 7, wherein the cache is configured as a write-back cache with a timeout flush.

12. The cache of claim 7, wherein the parity bit memory stores a single parity bit for each cache line in the data store.